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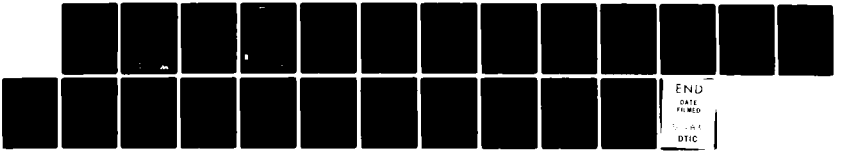

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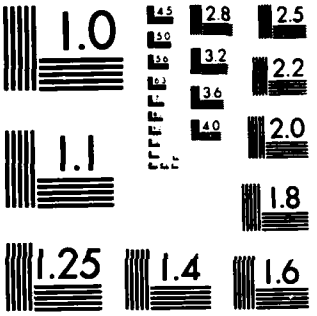

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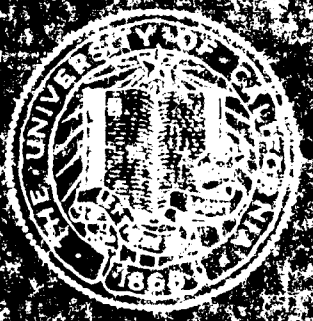

DESIGN AND IMPLEMENTATION OF MULTI-INPUT ADAPTIVE SIGNAL EXTRACTORS - FINAL REPORT

by

William A. Gardner and Michael A. Soderstrand

SIPL-82-12

September 1982

This work is supported by the United States Air Force Office of Scientific Research under Grant AFOSR-80-0189

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ABSTRACT

This is the Final Report on USAF grant AFOSR-80-0189 for the period June 1, 1980 through May 31, 1982 (extended to July 31, 1982). It covers research on design and implementation of novel adaptive digital signal processors for signal extraction (i.e., reduction of noise, interference, and distortion). The signal extractor configurations and adaptive adjustment schemes considered are extensions and generalization of prior art (viz., the FIR digital filter and the LMS adjustment algorithm) that consist of various combinations and interconnections of conventional adaptive filtering and noise cancelling configurations and associated adaptive adjustment schemes. The methods of implementation considered are based on speed-cost efficient Residue Number System arithmetic, and include Read Only Memory table look-up, and microprocessors and minicomputers for hardware control and for software implementation.

The major goals of the research are improvements over prior art in signal extraction performance (as measured by signal distortion, signal-to-noise ratio, and mean squared error) and in the cost of implementation and speed of operation. Results on design, implementation, and performance of configurations and adjustment schemes are described.

I-1 BRIEF STATEMENT OF OBJECTIVES FOR PART 1 OF PROJECT

1-1. Design/Analysis/Simulation of two-stage adaptive systems (networks), in which the basic component is an adaptive linear combiner; with applications to communications and signal processing systems including interference rejection (for ECCM and multi-user systems), signal distortion reduction (for channel equalization, and multi-sensor-arrays), noise filtering and cancelling, and system identification.

1-2. Design/Analysis/Simulation of multi-stage pilot-directed adaptive systems (for filtering, equalization, cancellation, and antenna null-steering and beam-forming), in which the pilot signal is a superimposed (or time-interleaved) periodically repeated pseudo-noise sequence; with applications to communications and signal processing systems as described in item 1 above.

1-3. Design/Analysis/Simulation of rapidly converging algorithms for adaptive estimation, based on novel computationally-efficient self-orthonormalization procedures (which are potential competitors with the fast recursive least squares (RLS) algorithms, but are not limited to the same class of estimation problems for which the RLS algorithms realize their computational efficiency; with applications including communications and signal processing systems as described in items 1 and 2 above.

1-4. Analysis/Simulation of dynamic adaptation in nonstationary environments, using newly refined methods for mathematical analysis of dynamic misadjustment due to the two fundamental sources, viz., tracking lag and stochastic measurements (e.g., "gradient noise"); with applications including communications and signal processing systems as described in items 1,2,3 above.

Items 1 and 2 are continuations (including extensions and generalizations) of our research carried out during the first two years of support from AFOSR; whereas items 3 and 4 were added in the third and final year of support.

I-2 RESULTS ON PART 1 OF PROJECT

2-1. Two-Stage Configurations for Adaptive Noise Cancellation

We have carried out theoretical analysis and simulations of two two-stage configurations, in which the first stage cancels noise (but introduces signal distortion due to signal leakage into the noise reference), and the second stage reduces distortion (introduced by the first stage). The first two-stage configuration is designed for intermittent signal (or signal-strength) applications [I-1], [I-2]; the second two-stage configuration is designed for slowly varying (relative to noise fluctuations) signals [I-2], [I-3]. Much of what was learned in this first study was applied to the investigations reported in the following items.

2-2. Pilot-Directed Adaptation

2-2-1. Simultations of three-stage configurations for dual-channel equalization, and noise and interference cancellation. Each of the two basic configurations described in references [I-4], [I-5], [1-6] admit several options including the optional versions of the recursive-like stage described in [I-7], [I-8], [I-9]. Both idealized analysis and computer simulations have been performed to evaluate and compare these various three-stage configurations. The results are promising, and are reported at length in [I-10], which shall be submitted under separate cover. In brief, the two basic configurations can be powerful signal extractors. The results indicate that the three stage configurations are capable of extracting an information bearing signal transmitted with a pilot signal. Noise can be cancelled, distortion introduced via transmission or the noise canceling stage can be removed, and the information bearing signal can be separated from the pilot signal. The simulations show typical improvements in the mean square error by factors of 5 to 75. Using

a signal-to-pilot power ratio (SPR) less than or equal to 0 dB, as discussed below, leads to improvements by factors of 20 to 75.

Although the idealized analysis suggests that signal extraction is possible regardless of the signal to pilot power ratio (SPR), simulations show that the SPR can be important. Simulations indicate that for best performance the power of the pilot should match or exceed the power of the information bearing signal. When the SPR is 0 dB or less the configurations are able to make use of the strong pilot signal to accurately adapt the filters to their optimum states. There appears to be no difference in the improvement between SPR's equal to 0 dB and -20 dB for configuration I, while for configuration II the smaller SPR provides greater improvement. This is attributed to the dependence on the pilot signal for adaptation of configuration II's second and third stages. Configuration I's second stage does not use the pilot to remove distortion while configuration II uses the pilot signal to direct the adaptation of the second stage (and hence also the third stage). As the power of the pilot is increased, the second stage is able to perform better. Although significant reduction of the mean square error is possible with a small pilot signal, the transmitted pilot tends to be masked by the signal (which is viewed as interference) from the replica stored at the receiver. (If a SPR greater than 0 dB is desirable, gradient averaging can be used to reduce the misadjustment.)

Important observations necessary for successful application of configurations I and II were made. First, there is a nonlinear dependence between the two filters in the dual-input filter/canceller which complicates choosing proper step sizes μ_{11} and μ_{12}. Second, the behavior of one stage will influence the behavior of subsequent stages. This makes the first observation even more critical. Properly choosing μ_{11} and μ_{12} for good noise cancelling performance is not highly critical, but carefully choosing μ_{11} and μ_{12} can improve the overall

mean square error performance. The second observation seems to be a result of nonstationarities in the inputs. The behavior of single stage filters and cancellers has long been studied when the input data is stationary. It is known how the magnitude of the step size parameter in adjustment algorithms affects the rate of convergence and final misadjustment. Larger step sizes yield increased rates of convergence but also larger final misadjustment, while smaller step sizes yield smaller final misadjustments but also decreased rates of convergence. In multi-stage configurations fast convergence would seem desirable so that input data to successive stages would be at a steady state. However, misadjustment is not only a measure of how close the converged result is to the desired output, but also an index of the amount of random fluctuations about the converged result. Large misadjustments are indicative of large random fluctuations in the output, which in the multi-stage case are the inputs to following stages. Thus, although the misadjustment for a particular stage may seem appropriately small, it may be large enough to produce a noticeable nonstationary input for the following stage.

While this study has addressed a number of issues, many more deserve consideration. More analysis of the dual-input noise/canceller needs to be done to understand the nonlinear dependence of the two filters so that good step sizes can hopefully be determined in advance of operation. Also, analysis of the effects of one stage on subsequent stages might provide a method for choosing good step sizes for the second and third stages. Additional work is necessary to fully explore the effect of the SPR on performance. Additional simulations involving more complex input data models (e.g. signals with non-flat power spectral densities and non-unity transformations G_1 and H_1) are necessary to determine the capabilities and differences of configurations I and II.

2-2-2. Extension from dual-channel environment to multi-channel environment, with application to adaptive antenna arrays. As described in references [I-4], [I-11], [I-12], the three stage configurations for dual-channel adaptive signal extraction, [I-4], [I-5], [I-6], can be generalized for multi-channel problems such as adaptive antenna arrays. In particular, in the first generalized configuration, [I-12], the first stage provides adaptive beam-forming and channel qualization (without knowing the desired signal strength or angle of arrival); the second stage cancels interference (without knowing interfering signal strengths or angles of arrival) by providing adaptive null-steering; and the third stage cancels the pilot that was used in the first two stages. In the second generalized configuration, [I-4], [I-11], the first stage provides both beam-forming and null-steering, but introduces some signal distortion; the second stage cancels the pilot used in the first stage, and in the process learns the signal distortion; the third stage then removes the signal distortion.

Our major effort in studying these multi-stage configurations for multi-channel environments went into detailed analysis for general application and for specific sensor array problems, and is reported at length in [I-11]. Briefly, it is shown that these adaptive systems can perform nearly as well as optimum linear systems designed on the basis of known signal, noise, and interference autocorrelation functions and spectral densities, provided that the transmission nulls in the channels are not too deep, and that receiver noise is sufficiently low. These general results are demonstrated for a simple two-input antenna array. Performance is graphed as a function of interference angle-of-arrival, for a fixed angle-of-arrival of a desired signal, and a variety of interference and receiver noise levels are considered. Performance is shown to be good as long as angles-of-arrival of interference and desired signal are not too similar.

2-2-3. Delayed-error pilot-directed adaptation. We have invented several multi-stage configurations for single-channel, dual-channel, and multi-channel (array) environments, that exploit a periodically repeated pseudo-noise pilot signal, by delaying the error signal used for adaptation by at least one period of the pilot. This renders all signals, noises, and interferences, with the exception of the pilot, that are in the adaptive filter, uncorrelated with same in the error, thereby putting the pilot in strong control of the adaptation. These most recently invented schemes are reported in [I-12], [I-13], [I-14].

2-3. Rapidly Converging Computationally Efficient Algorithms for Adaptation. Several new algorithms for adaptation have been developed as follows: A multiplication-free quantized-state, stochastic approximation algorithm for inverse correlation matrix estimation is imbedded in a deflected-stochastic-gradient-descent algorithm to obtain an N-dimensional, quasi-orthonormalized (deflected gradient) algorithm requiring only N+1 multiplications per adaptation step. Additional quantization is introduced to eliminate all multiplications. Simulations of an adaptive equalizer reveal that the new algorithm can yield substantially faster convergence than that of a non-deflected stochastic gradient (LMS) algorithm, but slower convergence than that of a recursive least squares (RLS) algorithm which, by design, exhibits the fastest possible speed of convergence. Also, the multiplication-free stochastic-approximation algorithm is imbedded in a deflected-projection algorithm to obtain an efficient algorithm for linearly constrained adaptive estimation. For applications, such as fully adaptive narrowband sensor array processing, the RLS algorithms cannot be implemented efficiently (because data vector elements do not shift sequentially through the vector); i.e., they require on the order of N^2 (rather than N) multiplications, per adaptation step. For such applications, the new algorithms are attractive alternatives to the slower LMS algorithm and the less efficient RLS algorithms. These results are reported at length in [I-15].

2-4. Analysis of Dynamic Adaptation in Nonstationary Environments.

In this research, probabilistic analysis or learning characteristics of the class of stochastic-gradient-descent algorithm for adapting the parameters of a non-recursive linear filter in order to identify a time-varying system from noisy measurements was carried out. Characteristics analyzed include stability, rate of convergence, steady state average and RMS misadjustments, average- and RMS-optimum adaptation step sizes, and sensitivity. A measure of the degree of nonstationarity for the system to be identified was proposed and its effects together with the effects of gradient-averaging, adaptation step size, and signal-to-noise ratio, on the learning characteristics were studied. The tracking performance of this class of algorithms was studied for the case in which the unknown system evolves according to (i) a first-order Markov random process and (ii) a periodic process. Simulation that verified the accuracy of the theoretical performance predictions were carried out. The results of this work are reported at length in [I-16].

I-3. PUBLICATIONS AND PRESENTATIONS OF RESULTS ON PART 1

I-1 W. A. Gardner and B. G. Agee, "Two-stage adaptive noise cancellation for intermittent-signal applications," IEEE Trans. Information Theory, Vol. IT-26, Nov. 1980, pp. 746-750.

I-2 J. Kazakoff and W. A. Gardner, "Simulations of two-stage adaptive signal extractors," 1981 Intern. Symp. on Information Theory, Santa Monica, California, Feb. 1981.

I-3 W. A. Gardner, "Two-stage adaptive noise cancellation for slowly fluctuating signals," Proc. IEEE, April 1981, Vol. 69, p. 487.

I-4 B. G. Agee and W. A. Gardner, "Embedded pilot signals for adaptive signal extraction in multi-channel environments," 1981 Intern. Symp. on Information Theory, Santa Monica, California, Feb. 1981.

I-5 W. A. Gardner, "Three-stage adaptive noise cancellation for arbitrary signals using an embedded pseudo-noise pilot signal, method I," Proc. IEEE, Vol. 69, No. 7, July 1981, pp. 848-849.

I-6 W. A. Gardner, "Three-stage adaptive noise cancellation for arbitrary signals using an embedded pseudo-noise pilot signal, method, II," Proc. IEEE, Vol. 69, No. 7, July 1981, pp. 849-850.

I-7 W. A. Gardner, "A stable two-stage recursive-like adaptive noise canceller," Proc. IEEE, April 1981, Vol. 69, pp. 487-488.

I-8 W. A. Gardner, "A soft-constrained recursive-like adaptive noise canceller," Proc. IEEE, April 1981, Vol. 69, pp. 488-489.

I-9 W. A. Gardner, "Cascade configurations for recursive-like adaptive noise cancellation," Proc. IEEE, July 1981, Vol. 69, pp. 846-847.

*I-10 P. L. Kelly and W. A. Gardner, "Pilot-Directed Adaptive Signal Extraction," Dept. of Electrical and Computer Engineering, Signal and Image Processing Lab Tech. Rept. No. SIPL-82-10.

*I-11 B. G. Agee and W. A. Gardner, "Embedded pilot signals for adaptive signal extraction in multi-channel environments," Dept. of Electrical and Computer Engineering, Signal and Image Processing Lab Tech. Rept. No. SIPL-82-11.

I-12 W. A. Gardner, "A pilot-directed adaptive beam-and-null steering processor for sensor arrays with accessible desired-signal sources," in revision for publication.

I-13 W. A. Gardner, "Pilot-directed joint channel-equalization/interference cancellation for multi-user multi-channel communication systems," in revision for publication.

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*Items marked with * are being submitted to AFOSR under separate cover. All others have been submitted in the past.

I-14 W. A. Gardner, "Fast recursive-like adaptive equalization for general-purpose communication channels," in revision for publication.

*I-15 W. A. Gardner and W. A. Brown, "State-quantized self-orthonormalized algorithms for rapidly converging computationally efficient adaptive estimation," Dept. of Electrical and Computer Engineering, Signal and Image Processing Lab Tech. Rept. No. SIPL-82-3.

*I-16 M. Hajivandi and W. A. Gardner, "Tracking performance of stochastic gradient algorithms for non-stationary processes," Dept. of Electrical and Computer Engineering, Signal and Image Processing Lab Tech. Rept. No. SIPL-82-9.

*Items marked with * are being submitted to AFOSR under separate cover. All others have been submitted in the past.

II-1 BRIEF STATEMENT OF OBJECTIVES FOR PART 2 OF PROJECT

1-1. Microprocessor Controlled Adaptive Filter Development System (MCAFDS)

The MCAFDS consists of two separate pieces of hardware. One is a specially designed RNS multiplier/accumulator which may be placed in an S-100 bus to allow software configuring to implement both IIR and FIR digital filters with 8-bit I/O signals. The second piece of hardware is an adaptive update board for implementing adaptive filters with various algorithms. The goals of this project were:

1a. Design, analyze and simulate RNS multiplier/accumulator hardware.

1b. Design, analyze and simulate adaptive update hardware.

1c. Build, test and evaluate RNS multiplier/accumulator hardware.

1d. Build, test and evaluate adaptive update hardware.

1-2. Microprocessor Controlled Totally Adaptive Filter (TAF)

The TAF consists of microprocessor controllable hardware which may be configured by software to implement FIR and various IIR digital filters. Through software, the TAF will adapt structure as well as weights. The goals of this project were:

2a. Design, analyze and simulate the TAF hardware.

2b. Investigate possible structure searches.

2c. Investigate optimum initialization.

2d. Investigate possible applications.

1-3. RNS Sign-Detection and Magnitude-Estimation Hardware

The hardware proposed for this project consisted of a Chinese Remainder Theorem based RNS to binary converter that could be used for sign detection and magnitude comparison. The goals of this project were:

3a. Design, analysis and simulation of new Chinese Remainder Theorem hardware.

3b. Build, test and evaluate new Chinese Remainder Theorem hardware.

1-4. Design of Small Moduli RNS Adaptive Filter

The small moduli RNS adaptive filter consists of two hardware blocks. The basic FIR filter is a modulo 16, 15, 13, 11 RNS filter implemented with ROM table look-up hardware for 10 MHz operation. The second piece of hardware is an adaptive update board based on a slowed-down LMS algorithm simplified by truncation and saturation. The goals of this project were:

4a. Design, analyze and simulate the FIR RNS filter hardware.

4b. Build, test and evaluate the FIR RNS filter hardware.

4c. Design, analyze and simulate the adaptive update hardware.

4d. Build, test and evaluate the adaptive update hardware.

1-5. Multiple Microprocessor RNS Adaptive Filters

In this project separate microprocessors are used to implement large moduli adaptive FIR digital filters. Specific goals of the project were:

5a. Design, analysis and simulation of multiple microprocessor filter hardware.

5b. Design, analysis and simulation of appropriate update hardware.

5c. Build, test and evaluate multiple microprocessor filter hardware.

5d. Build, test and evaluate update hardware.

1-6. Implementation of a RNS FIR Digital Filter in Multiple Valued Logic (RNS-MVL Digital Filter)

The RNS-MVL Digital Filter is an RNS digital filter implemented in multiple valued logic. Goals of this project were:

5a. Development of a practical implementation of RNS moduli in MVL.

5b. Design, analysis and simulation of required RNS MVL circuit elements.

II-2 RESULTS ON PART 2 OF PROJECT

2-1. Microprocessor Controlled Adaptive Filter Development System (MCAFDS)

The MCAFDS is essentially completed. Complete details of the project are contained in two technical reports (II-29 and II-32). M.S. theses based in part on this project were submitted by Mr. David Paulson (M.S. 1982) and Mr. James Buteau (M.S. pending). Additional work on goal 1d below is currently being carried out by M.S. candidate Mr. Jeffrey Liong. Here is a breakdown of publications describing the achievement of each goal:

1a. Design, analysis and simulation of RNS multiplier/accumulator (II-5, II-14, II-25, II-29).

1b. Design, analysis and simulation of adaptive update hardware (II-17, II-29, II-32).

1c. Build, test and evaluate RNS multiplier/accumulator hardware (II-16, II-29).

1d. Build, test and evaluate adaptive update hardware (II-29, II-32).

2-2. Microprocessor Controlled Totally Adaptive Filter (TAF)

The TAF project goals are essentially complete, but considerable additional work is comtemplated. Ms. Celia Vigil (M.S. 1981) based her thesis on work performed on this project. Ms. Jana Kelley (M.S. expected 1983) and Mr. James Buteau (M.S. pending) both contributed to this work. Complete details of the preliminary work are contained in a technical report (II-26). Specific publications on each of the goals are listed below:

2a. Design, analysis and simulation of TAF hardware (II-8, II-10, II-11, II-22, II-23, II-26).

2b. Investigate possible structure searches (II-2, II-3, II-7, II-26).

2c. Investigate optimum initialization (II-22, II-23).

2d. Investigate possible applications (II-22, II-23, II-26).

2-3. RNS Sign-Detection and Magnitude-Estimation Hardware

This work is complete. Early work was done by Mr. Carmel Vernia (M.S. 1981) and was followed up by Ms. Connie Chang (B.S. 1982). Details are included in the technical reports (II-27, II-31). Publications related to each goal are as follows:

3a. Design, analysis and simulation of new Chinese Remainder Theorem hardware (II-1, II-13, II-24, II-27, II-31).

3b. Build, test and evaluate new Chinese Remainder system hardware (II-24, II-27, II-31).

2-4. Design of Small Moduli RNS Adaptive Filter

This project is nearly complete. Two technique reports detail much of the work (II-39 and II-31). Ms. Kim Weinman (M.S. 1982) and Ms. Jana Kelley (M.S. expected 1983) based much of their M.S. work on this project. Ph.D. candidate Soliman Shebani is in the process of completing the remaining work on this project. In addition, Ms. Connie Chang (B.S. 1982) and Mr. Jeff Wong (B.S. 1982) worked on aspects of this project. Detailed publications are as follows:

4a. Design, analysis and simulation of FIR RNS filter hardware (II-12, II-15, II-31).

4b. Build, test and evaluate FIR RNS filter hardware (II-31).

4c. Design, analysis and simulation of adaptive update hardware (II-12, II-15, II-17, II-18, II-20, II-30).

4d. Build, test and evaluate the adaptive update hardware (II-30).

2-5. Multiple Microprocessor RNS Adaptive Filters

The analysis and simulation protions of this project are complete. A technical report details the project (II-27), hardware construction is

continuing. Specifically,

5a. Design, analysis and simulation of multiplier microprocessor filter hardware (II-4, II-5, II-6, II-9, II-14, II-21, II-27).

5b. Design, analysis and synthesis of appropriate update hardware (II-9, II-21 II-27).

5c. Build, test and evaluate multiplier microprocessor filter hardware (II-27).

5d. Build, test and evaluate update hardware (II-27).

2-6. Implementation of a RNS FIR Digital Filter in Multiple-Valued Logic

Work is still continuing on this project but much has been accomplished and will be described in a technical report (II-33). Specific publications are:

5a. Development of a practical implementation of RNS moduli in MVL (II-19, II-33).

5b. Design, analysis and simulation of required RNS MVL circuit elements (II-19, II-33).

II-3. PUBLICATIONS AND PRESENTATIONS OF RESULTS ON PART 2 OF PROPOSAL

(Note: The following list contains all articles published in both year 1 and year 2 of the project.)

II-1 M. A. Soderstrand, "High-speed data conversion using residue number arithmetic A/D and D/A converters," Proc. 22nd Midwest Symposium on Circuits and Systems, Philadelphia, PA, June 1979, pp. 6-10.

II-2 M. A. Soderstrand, "Adaptive Recursive Filters," Proc. 1979 Intern. Colloquium on Circuits and Systems, Taiwan, China, July 1979.

II-3 M. A. Soderstrand, "Cost and Performance Comparisons of Several Implementations of Adaptive Recursive Filters," Proc. 13th Asilomar Conference on Circuits, Systems and Computers, Pacific Grove, CA, Nov. 1979, pp. 416-420.

II-4 M. A. Soderstrand and C. Vernia, "A high-speed low-cost modulo P. multiplier with RNS arithmetic applications," Proc. IEEE, Vol. 68, No. 4, April 1980, pp. 529-532.

II-5 M. A. Soderstrand, C. Vernia, D. W. Paulson and M. C. Vigil, "Microprocessor controlled adaptive digital filters," Proc. IEEE Intern. Symposium on Circuits and Systems, Houston, TX, April 1980, Vol. 1, pp. 192-196.

II-6 M. A. Soderstrand and C. Vernia, "General modulo P. multiplier with RNS arithmetic applications," Proc. IEEE Intern. Symposium on Circuits and Systems, Houston, TX, April 1980, Vol. 3, pp. 1121-1124.

II-7 E. L. Fields and M. A. Soderstrand, "Performance characteristics of digital ladder networks," Proc. IEEE Intern. Symposium on Circuits and Systems, Houston, TX, April 1980, Vol. 3, pp. 1121-1124.

II-8 M. A. Soderstrand and M. C. Vigil, "Simulation studies of a totally adaptive digital filter," Proc. 23rd Midwest Symposium on Circuits and Systems, Toledo, Ohio, August 1980.

*II-9 M. A. Soderstrand and C. Vernia, "Microprocessor controlled development system for adaptive filtering using parallel processing and residue number arithmetic," ISMM Intern. Symposium on Mini and Micro Computers, Montreal, Canada, September 1980.

II-10 M. A. Soderstrand and M. C. Vigil, "Microprocessor controlled totally adaptive filter," 1980 IEEE Intern. Conference on Circuits and Computers, Agetown, New York, October 1980.

*II-11 M. A. Soderstrand, J. K. Kelley and J. J. Buteau, "A microprocessor based RNS arithmetic totally adaptive digital filter for system identification," 14th Asilomar Conference on Circuits, Systems and Computers, Pacific Grove, CA, November 1980.

* II-12 M. A. Soderstrand and J. K. Kelley, "Design of a low-cost adaptive FIR filter with sampling rate in excess of 10mhz," 1981 IEEE Intern. Symposium on Circuits and Systems, Chicago, IL, April 1981.

* II-13 M. A. Soderstrand and C. Vernia, "An improved RNS digital-to-analog converter," 1981 IEEE Intern. Symposium on Circuits and Systems, Chicago, IL, April 1981.

* II-14 M. A. Soderstrand, "Techniques for Computer-Based Digital Signal Processing," ISMM Intern. Symposium on Mini and Microcomputers in Control and Measurement, San Francisco, CA, May 20-22, 1981.

* II-15 M. A. Soderstrand, "New Hardware for High-Speed Adaptive Digital Filtering," 24th Midwest Symposium on Circuits and Systems, Albuquerque, NM, June 1981.

* II-16 M. A. Soderstrand, "Experimental Results From a Microprocessor-Based Digital Filter Designed for Brainwave Monitoring," ISMM Intern. Symposium on Mini and Microcomputers, Cambridge, MA, July 7-9, 1982.

* II-17 M. A. Soderstrand, M. C. Vigil, J. J. Buteau and J. K. Kelley, "Experimental Performance Data for Slowed-Down Adaptive Algorithms," Intern. Journal of Electronics, Vol. 53, No. 1, July 1982.

* II-18 K. D. Weinmann and M. A. Soderstrand, "Influences of Hardware Implementation on a High-Speed Digital Adaptive Filter Using the Residue Number System," 25th Midwest Symposium on Circuits and Systems, Houghton, MI, August 1982.

* II-19 R. A. Escott and M. A. Soderstrand, "Application of Multiple-Valued Logic to Residue Number System Computation," 25th Midwest Symposium on Circuits and Systems, Houghton, MI, August 1982.

* II-20 K. D. Weinmann, M. A. Soderstrand and S. Shebani, "Evaluation of New Hardware for High Speed Adaptive Digital Filters Using the Residue Number System," (to be published 1982 Asilomar Conference, Pacific Grove, CA, November 1982).

* II-21 M. A. Soderstrand and C. Vernia, "Microprocessor controlled development system for adaptive filtering," Intern. Journal of Mini and Micro Computers, (to be published).

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*Items marked with * are being submitted to AFOSR under separate cover. All others have been submitted in the past.

III PROFESSIONAL PERSONNEL ASSOCIATED WITH THE RESEARCH EFFORT

3-1. Senior Personnel

1. William A. Gardner - Principal Investigator
   Professor

2. Michael A. Soderstrand - Principal Investigator
   Associate Professor

3-2. Student Personnel

1. Brian G. Agee (M.S. pending)

2. Phillip Kelly (M.S. June 1982)
   Thesis Title: Pilot-Directed Adaptive Signal Extraction and Rapidly-Converging Computationally-Efficient Algorithms

3. James Kazakoff (M.S. pending)

4. Mehrdad Hajivandi (Ph.D. June 1982)
   Thesis Title: Tracking Performance of Stochastic Gradient Algorithms for Nonstationary Processes

5. William A. Brown (Ph.D. candidate)

6. Carmel Vernia (M.S. June 1980)
   Thesis Title: Multi-Microprocessor Non-Recursive Adaptive Digital Signal Processing Using Residue Number Arithmetic

7. M. Celia Vigil (M.S. June 1980)
   Thesis Title: A Totally Adaptive Filter

8. David W. Paulson (M.S. December 1981)
   Thesis Title: Microprocessor Controlled Adaptive Digital Filtering Using Residue Number System Multiplier/Accumulator and Filter Weight Adjustment Modules

9. Kimberly D. Weinmann (M.S. April 1982)
   Thesis Title: Influences of Hardware Implementation on a High-Speed Digital Adaptive Filter Using Residue Number System

10. James J. Buteau (M.S. expected Winter 1983)
    Thesis Title: Microprocessor Based Digital Adaptive Filters

11. Jana K. Kelley (M.S. expected June 1983)
    Thesis Title: Adaptive FIR Filter with 10MHz Sampling Rate

12. Richard A. Escott (M.S. expected March 1983)
    Thesis Title: Implementation of RNS Digital Filters in Multiple-Valued Logic

13. Jessy Lawrendra (M.S. candidate)

14. Soliman Shebani (Ph.D. candidate)